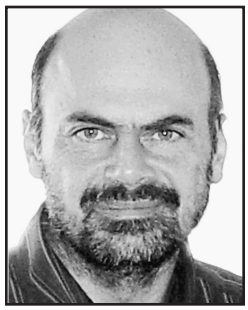
Session 25 Overview

Nyquist ADC Techniques



Chair: Dieter Draxelmayr, *Infineon Technologies, Villach, Austria*

Associate Chair: Venu Gopinathan, *Texas Instruments, Bangalore, India*

Many applications like video data conversion, fast communication services, and direct IF conversion require medium resolution A/D converters, sampling in the range of a few 100MHz. The pipelined-converter technique offers an attractive implementation possibility. Consequently, in this session there are 6 examples demonstrating the current state-of-the-art in this category. Advances are characterized mostly in getting highly power-optimized solutions. Most designs are implemented in state-of-the-art 90nm technologies. While this helps to get good performance it also poses the challenge of low power supplies.

Obviously, another direction of advancing the state-of-the-art is to go for extreme performance. In this session there will be two examples: A 50GS/s T/H amplifier, which can be used for direct conversion of a 40Gb/s signal from an optical link including even slight oversampling. This can be used to boost the performance of such a link in enabling advanced equalization techniques. The second example is a cryogenic ADC that can operate at the temperature of liquid helium, which is a major step forward in low-temperature readout electronics.

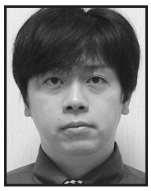
The nine presentations of this session are grouped as follows: the first 7 papers demonstrate the current capabilities in medium-resolution high-speed low-power applications. The last 2 papers demonstrate benchmark performance.

The converter in Paper 25.1 from Fujitsu demonstrates very low power consumption at a supply voltage of only 0.8V. The regulation of the gate overdrive voltage for optimizing the available voltage headroom is introduced as an enabling technique. The next paper, 25.2 from UCLA, attempts to perform the same precision of data conversion at twice the speed but using a sub-ranging architecture, operating at 1V. The converters proposed in Papers 25.3 from ETRI and 25.4 from ETRI and LG Electronics use 3b pipeline stages to achieve 10b precision at 30MS/s and 205MS/s sampling rate, respectively. The faster one needs a S/H in front of the converter.

The authors of Paper 25.5 from MIT present an 8b 200MS/s pipelined converter implemented in a just recently invented circuit technology which does not need active amplifiers. This promises another boost in power saving since opamps usually are the most power-hungry parts in an ADC. Papers 25.6 from Nordic Semiconductor and 25.7 from Realtek and UCLA improve the performance in using foreground and background calibration. Foreground calibration is used for a fast power-up, and after that, background calibration ensures adequate performance over time.

The authors of Paper 25.8 from Lucent present a 50GS/s T/H amplifier in SiGe technology. This benchmark in speed is achieved using a distributed topology, a technique well known in high-speed amplifiers, here applied to track-and-holds.

Finally, Paper 25.9 from IMEC and KU Leuven discusses a SAR ADC that can work from room temperature down to 4.2K. The specifics in this paper are that at 4.2K the transistors work differently than what we are used to. Therefore, specific circuit techniques had to be adopted to cope with this challenge.



25.1 A 0.8V 10b 80MS/s 6.5mW Pipelined ADC with Regulated Overdrive Voltage Biasing **8:30 AM**

M. Yoshioka, Fujitsu, Kawasaki, Japan

A low-voltage design is developed for amplifiers in the pipelined ADC, regulating overdrive voltage to be constant over PVT variations. A prototype 10b 80MS/s pipelined ADC is fabricated in a 90nm CMOS process. The ADC consumes 6.5mW from a 0.8V supply and occupies 1.18×0.54mm^2.

25.2 A 10b 160MS/s 84mW 1V Subranging ADC in 90nm CMOS **9:00 AM**

D. Huber, University of California, Los Angeles, CA

A 10b 160MS/s subranging ADC with THA is implemented in a 90nm digital CMOS process. Noise averaging and an auto-zeroed comparator are used in the fine converter to achieve low noise and offset at low power dissipation. The prototype converter achieves an ENOB of 9.1b for an 80MHz input and consumes 84mW from a 1V supply.

25.3 A 4.7mW 0.32mm^2 10b 30MS/s Pipelined ADC without a Front-End S/H in 90nm CMOS **9:30 AM**

Y-D. Jeon, Electronics and Telecommunications Research Institute, Daejeon, Korea

A 4.7mW 10b 30MS/s pipelined ADC is implemented without a front-end S/H for low power consumption and small area. The prototype ADC, fabricated in a 90nm CMOS process, shows an SNDR of 58.4dB and an SFDR of 75.2dB with a 2MHz sinusoidal input sampled at 30MS/s. The 0.32mm^2 chip dissipates 4.7mW at a 1V supply and has a FOM of 0.23pJ/conversion-step.

25.4 A 10b 205MS/s 1mm^2 90nm CMOS Pipeline ADC for Flat-Panel Display Applications **9:45 AM**

S-C. Lee, Electronics and Telecommunications Research Institute, Daejeon, Korea

A 10b 205MS/s 1mm^2 ADC for flat-panel display applications is implemented in a 90nm CMOS process. The ADC with an LDO regulator achieves a 53dB PSRR for a 100MHz noise tone and a 55.2dB SNDR for a 30MHz $1V_{pp}$ single-ended input at 205MS/s. The core ADC power consumption is 40mW from a 1V non-regulated supply.

25.5 A Zero-Crossing-Based 8b 200MS/s Pipelined ADC **10:15 AM**

L. Brooks, Massachusetts Institute of Technology, Cambridge, MA

A zero-crossing-based 8b 200MS/s pipelined ADC is implemented in a 0.18µm CMOS process. It uses dynamic zero-crossing detectors and digital FFs that replace the functions of opamps and comparators. The ADC draws no static current. The power consumption is 8.5mW. The FOM is 0.51pJ/step.

25.6 A 92.5mW 205MS/s 10b Pipelined IF ADC Implemented in 1.2V/3.3V 0.13µm CMOS **10:45 AM**

B. Hernes, Nordic Semiconductor, Trondheim, Norway

A 10b 205MS/s IF sampling pipelined ADC is fabricated in 1.2/3.3V 0.13µm CMOS. Power consumption and die area are improved by using single-stage opamps throughout the pipeline chain; digital calibration compensates for the reduced stage gain. Foreground calibration is used to shorten the start-up time and background calibration is used afterwards. The ADC has ENOB of 9.0, ERBW of 330MHz, dissipates 92.5mW, and occupies 0.52mm^2.

25.7 An 11b 800MS/s Time-Interleaved ADC with Digital Background Calibration **11:15 AM**

C-C. Hsu, Realtek, Hsinchu, Taiwan

An 11b 800MS/s time-interleaved ADC is implemented in a 90nm CMOS process for a 10GBase-T application. A single open-loop T/H circuit using a cascode source follower achieves high resolution and conversion rate. The offset and gain mismatches are corrected by the digital background calibration. The measured DNL and INL are <0.5LSB and <1.6LSB, respectively. The measured SNDRs are 58 and 54dB for 15 and 400MHz inputs, respectively. The 1.4mm^2 ADC consumes 350mW from a 1.3V supply (1.5V for T/H).

25.8 A 50GS/s Distributed T/H Amplifier in 0.18µm SiGe BiCMOS **11:45 AM**

J. Lee, Alcatel-Lucent, Murray Hill, NJ

A 3-stage distributed T/H amplifier (DTHA) is presented for high-bit-rate optical receivers and millimeter-wave radios. Distributed topology enhances the bandwidth of the DTHA to >42GHz in track mode. The DTHA achieves 2-tone SFDR of 46dB with 15GHz input signal. The 1.47mm^2 chip designed in a 0.18µm SiGe BiCMOS process dissipates 640mW.

25.9 A Cryogenic ADC Operating Down to 4.2K **12:00 PM**

Y. Creten, IMEC, Heverlee, Belgium, and KU Leuven, Heverlee, Belgium

A SAR ADC is designed to operate from room temperature down to 4.2K, as needed by cryogenic sensor systems. The ADC is robust to cryogenic temperature-induced transistor anomalies. It has an INL of -0.8(0.5)LSB and DNL of 1.1(0.4)LSB at 4.2K(300K). It draws 70µA for a 200pF output capacitor at 3kHz sampling rate and 5V supply.